UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,916	10/13/2004	Yin-Chang Chen	AMIP0030USA	5915

27765 7590 01/09/2006

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
JAGER, RYAN C	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,916	CHEN ET AL.	
	Examiner	Art Unit	
	Ryan C. Jager	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6 and 8* is/are rejected.

7)☒ Claim(s) *5,7,9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1 and 6 are rejected under 35 U.S.C. 103(a) as being anticipated by Sugimura (6456154) in view of Applicant's admitted prior art (Figure 1).

With respect to claim 1, figure 5 of Sugimura discloses a boost circuit capable of boosting a reference voltage (voltage at node 100) into an output voltage (voltage at node 200), a pre-charge circuit (ND1) and a voltage detector (CMP2). Figure 5 of Sugimura lacks a main and auxiliary transistor. However, figure 1 of the applicant's prior art discloses a capacitor formed from an NMOS transistor (14, figure 1 prior art; page 2, specification). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the circuit in figure 5 of Sugimura by replacing each of the capacitors (C1, C2, ..., Cn) with an NMOS transistors configured as a capacitor as shown in figure 1 of the prior art to function as a capacitor, for the purpose of producing a fully integrated circuit. The above modification discloses a main transistor (C1) electrically connected to the output voltage, an auxiliary transistor (C2) electrically connected to the output voltage, a pre-charge circuit (ND1) electrically connected to the main transistor (C1) and the auxiliary transistor (C2) for pre-charging the main transistor and the auxiliary transistor, and a voltage detector (CMP2)

electrically connected to the auxiliary transistor and the reference voltage for controlling the auxiliary transistor according to the reference voltage (voltage at node 100).

With respect to claim 6, figure 5 of Sugimura discloses a re-charge module (MP1) electrically connected to the main transistor (C1) for re-charging the main transistor.

2. Claims 2, 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugimura (6456154) in view of Applicants admitted prior art and further in view of Hung et al. (6100557).

With respect to claims 2 and 3, the above modification as discussed in claim 1 discloses all the limitations of these claims except that the main and auxiliary transistors are triple-welled NMOS transistors. However, Hung discloses that using triple-well transistors reduce the body effect of the transistor and allow the charge pump to operate more efficiently (abstract, pg 1). Therefore it would have been obvious to one skilled in the art at the time the invention was made to modify the circuit in figure 5 of Sugimura by replacing the main and auxiliary transistor with triple-welled NMOS transistors for the purpose of creating an efficient charge pump.

3. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being anticipated by Tomishima (5909141) in view of Applicant's admitted prior art (Figure 1).

With respect to claim 1, figures 1, 4 and 27 of Tomishima disclose a boost circuit capable of boosting a reference voltage (Vs, figure 4) into an output voltage (Vpp, figure 1), a pre-charge circuit (95 and 97) and a voltage detector (4, figure 1). Figures 1, 4 and 27 lack a main and auxiliary transistor. However, figure 1 of the applicant's prior art

discloses a capacitor formed from an NMOS transistor (14, figure 1 prior art; page 2, specification). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the circuit in figure 27 of Tomishima by replacing each of the capacitors (105, 107 and 109) with an NMOS transistor configured as shown in figure 1 of the prior art to function as a capacitor, for the purpose of producing a fully integrated circuit. The above modification discloses a main transistor (109) electrically connected to the output voltage, an auxiliary transistor (105) electrically connected to the output voltage, a pre-charge circuit (95 and 97) electrically connected to the main transistor (109) and the auxiliary transistor (105) for pre-charging the main transistor and the auxiliary transistor, and a voltage detector (4, figure 1) electrically connected to the auxiliary transistor and the reference voltage for controlling the auxiliary transistor according to the reference voltage (Vs, figure 4).

With respect to claim 4, figure 1, 4 and 27 disclose a boost circuit, wherein the voltage detector disables the auxiliary transistor (105 of figure 1) when detecting that the reference voltage (Vs, figure 4) is higher than a predetermined voltage (VR from 177, figure 4 and column 14, lines 1-15).

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ting et al. (6198340) in view of Applicant's admitted prior art (Figure 1).

With respect to claim 8, figure 2 of Ting et al. discloses a boost circuit capable of boosting a reference voltage (Vcc) into an output voltage, a pre-charge circuit (38), a main recharge transistor (37), and a stable recharge transistor (36). Figure 2 lacks a stable transistor and a main transistor. However, figure 1 of the applicant's prior art

discloses a capacitor formed from an NMOS transistor (14, figure 1 prior art; page 2, specification). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the circuit in figure 2 of Ting by replacing each of the capacitors (C1 and C2) with an NMOS transistor configured as shown in figure 1 of the prior art to function as a capacitor, for the purpose of producing a fully integrated circuit. The above modification discloses a main transistor (C2) electrically connected to the output voltage (Vout), a pre-charge circuit (38) electrically connected to the main transistor (C2) for pre-charging the main transistor, a stable transistor (C1), a main re-charge transistor (37) electrically connected between the stable transistor (C1) and the main transistor (C2) for re-charging the main transistor according to a voltage level of the stable transistor (C1), and a stable re-charge transistor (36) electrically connected between the stable transistor (C1) and the main transistor (C2) for re-charging the stable transistor (C1) according to a voltage level of the main transistor (C2).

Allowable Subject Matter

5. Claims 5, 7, 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan C. Jager whose telephone number is (571) 272-7016. The examiner can normally be reached on M-F 8 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan Jager
12-27-2005
RJ

LONG NGUYEN
PRIMARY EXAMINER